Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC

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Abstract:

We will describe a low cost and low power Si Bipolar IC for clock and data recovery at 2.488 Gb/s that requires no external reference. The design is based on a digital quadri-correlator that has inherent low phase offset and allows the use of passive loop filters. The clock recovery unit (CRU) has broad locking range that makes it robust against power supply and temperature variations.

Introduction

Using a 14 GHz Si bipolar process we have integrated a CRU for the Synchronous Optical Network (SONET) communication standard OC-48 (optical carrier at 48 times base frequency). Our IC consumes a modest 0.8 W while performing the functions of recovery, re-timing and lock detection. It is based on a phase-locked loop (PLL) which contains a digital frequency and phase detector (DFPD), known as a digital quadri- correlator, that can extract the information from the incoming data without requiring an external clock reference for frequency acquisition.

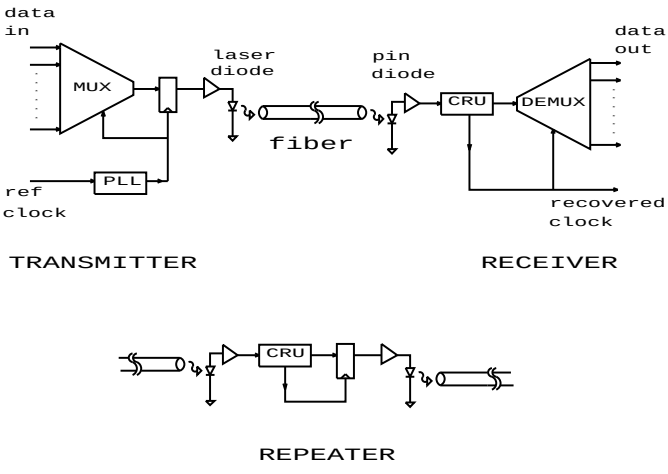

Figure 1: Optical data transmission system

System overview

Shown in Fig. 1 is a simplified overview of an optical fiber data communications system. The transmitter needs to originate the data at high serial rate (for example 2.488 Gb/s) and consists of a multiplexor and a PLL used for synthesis. The receiver must recover the clock, re-time the data and de multiplex it [1,2]. Additionally, systems use many repeaters, which consist of optical interfaces and clock recovery and data retiming. The specifications for the repeater are the most difficult since they must balance not only transfer, tolerance and generation of jitter, but limited power consumption and robust design against environmental changes in voltage supply and temperature.

IC block description

A simplified IC block diagram is shown in Fig. 2. The incoming data is compared against the internal voltage controlled oscillator (VCO) in the DFPD. Its output is differentially filtered and applied to the oscillator. The reference input is required only for the lock detector, where it is compared against the VCO divided by 16. The data is re-timed by a d-flip-flop, using the inverted in phase VCO clock output. This CRU consists of fewer building blocks than one that requires a reference and a dual-loop PLL.

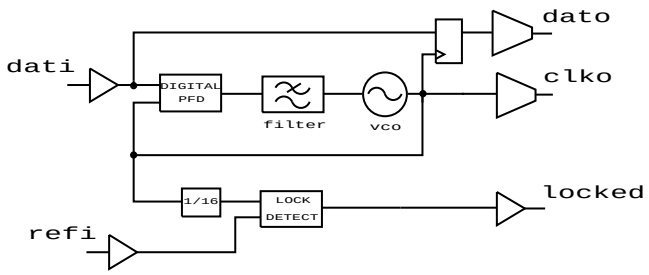

Figure 2: CRU Block Diagram

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Voltage Controlled Oscillator

Our VCO, a two stage ring oscillator, is shown in Fig. 3. It consists of a slow and a fast amplifiers that are parallel connected. Their “tail” current is controlled by a third differential amplifier. When this current is divided between the slow and fast amplifiers, a middle delay is obtained. Emitter followers isolate, buffer and speed up the oscillator stages. The tuning range of our VCO is from 2.3 to 2.7 GHz, and it provides quadrature outputs (90 degrees out of phase). These outputs are required for the digital quadri-correlator.

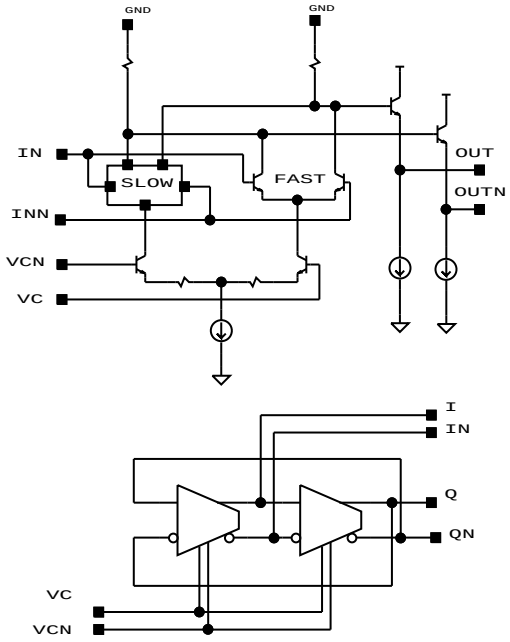

Figure 3: Two stage ring-oscillator VCO.

Digital Quadri-correlator

The digital quadri-correlator (or DFPD), shown in Fig. 4, consists of 2 dual-edge triggered flip-flops, logic circuitry for determining relative frequency, and summing circuitry that produces control signals for VCO. In-phase and quadrature output of VCO are sampled on the rising and falling edges of the data signal to produce the signals Q1 and Q2. By observing the relative phase of Q1 and Q2, Q3 is derived and it indicates the relative frequency of VCO compared to the DATA signal. Control signals for VCO are generated subsequently from the summing circuitry [3, 4]. Once in locked condition, Q1 operates in a “bang-bang” mode as a phase detector, while Q2 remains low indicating inactivity of the frequency loop. Lock detection is indicated by Q2, and, therefore, a separate lock detection circuitry is not required in principle.

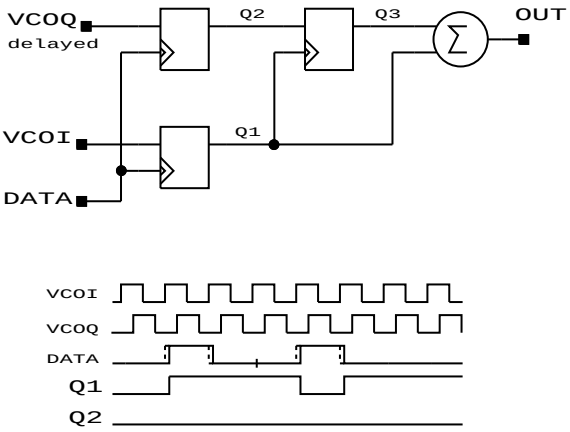

Figure 4: Digital Frequency and Phase Detector.

Loop design

The loop filter is entirely passive consisting only of resistors and capacitors, and it requires no op-amp. It is fully integrated except for one external chip capacitor. The inherent low phase offset of the DFPD, due to the high gain of the "bang-bang" phase detector, allows this simple filter which consumes less power and provides better loop stability since no higher order poles exist as when an op-amp is used.

Heavily damped loop response is desired in order to keep the peaking in the pass-band to less than 0.1 dB as required in the OC-48 specification. The loop bandwidth of a heavily damped system is proportional to the open loop gain. The gain of the VCO tends to be large, in order to have enough tuning range for a given range of control voltage. The high VCO gain will, unfortunately, make the loop bandwidth too wide. This situation is further compounded by the "bang-bang" phase detector which has large gain itself. Hence, a network of resistor divider and a large 1uF external capacitor are used to reduce the gain of the AC component of the control voltage before it is applied to the VCO. The resistor divider network is designed to make the loop response stable with 3 dB frequency of about 1.1 MHz.

A behavioral model in the phase domain, shown in Fig. 5, is extensively used to verify the stability of the PLL. Although the model is single ended and the circuit is actually implemented in a differential architecture, it should be equivalent in terms of predicting the loop stability. Controlled sources are used to model the phase detector and the VCO. The "bang-bang" characteristic of these PFDs are highly non-linear. However, the simplified circuit shown could be used by adjusting the gain and the clamp level of KP. To verify the large signal loop bandwidth (i.e., jitter tolerance), we run transient analysis with sinusoidal inputs of varying amplitude and frequency. KV models the gain of the VCO. A 1 ohm resistor and a 1 F capacitor sim-

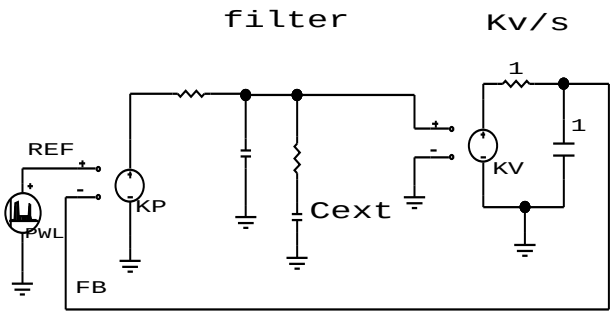

Figure 5: Simplified loop stability model

ulate an ideal integrator which is needed to model the VCO in the phase domain.

Lock Detector

The lock detector shown in Fig. 6 works as a relative frequency measuring system. It determines if an optional reference and the internally divided down VCO are different by more than a preset percentage. The basis of its operation is the generation of a beat frequency between the two inputs, by the use of two flip-flops. This beat signal enables a counter that counts either the reference or the VCO divided by 16. If the two inputs are close in frequency, then a high count will occur during the beat signal high state. Then the counter will "carry" and disarm a trip point set by the beginning of the beat waveform.

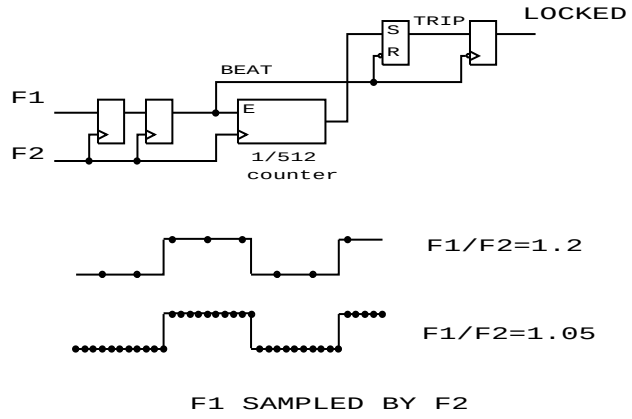

Figure 6: Lock Detector.

Input and Output Buffers

At the operating frequency of the circuit, integrity of input and output signals may easily be compromised by package and bonding inductance. Thus, input and output buffers are internally terminated with on chip 50 ohm resistors to minimize ringing caused by reflections. Input buffers are also internally self biased to accommodate AC coupling. Output buffers are open collector with internal load, and can provide 300mV DC swing into external 50 ohm load. The current densities in the emitter follower stages prior to output buffers are adjusted in order to reduce ringing [5].

Test set-up

The ICs were packaged in a plastic thin quad flat package (TQFP) to minimize the lead inductances at the outputs, the loop filter external pins and the power buses. A rough estimate of inductance for our package is 5 nH per pin. The effect of this uncontrolled "impedance" is lessened by using inputs and outputs that are 50 ohm terminated on-chip.

The evaluation board had to be carefully designed. Several iterations of both two layer and four layer boards have been necessary to optimize the output waveforms for the data (2.5 Gb/s) and the clock (2.5 GHz). It is easy to handle these frequencies inside the chip, but difficult to cross the package barrier. Therefore it may be desirable, in the future, to not bring them out but rather to do de-multiplexing on chip.

The measurement of SONET specifications requires the use of special test equipment designed for this purpose, commonly known as bit-error-rate-tester (BERT). It is capable of injecting data with different pseudo random patterns with varying amounts of jitter, and to verify the correctness of the recovered data and the amounts of jitter present at the output.

Measured Performance

Table 1 below summarizes the measured performance of the clock and data recovery IC. The jitter generated by our IC

Table 1: Summary of measured performance parameters

Specification or parameter	Measured Value
Jitter generation	2.9 pS rms
Jitter transfer	peaking < 0.03 dB 3 dB corner 1.1 MHz
Jitter tolerance	Meets with 25% overdrive
Lock range	2.4 -2.6 GHz
Operating temperature	-40 to +85 C (industrial)
Operating voltage	4.75 to 5.25 V
Power consumption	0.8 W

is typically about 2.9 pS rms, and this meets the SONET specification of 4 pS rms [2]. The jitter transfer specification measures the input to output transfer function of the part, and is equal to one (with less that 0.1 dB peaking) up to a maximum band edge frequency. Fig. 7 shows the jitter transfer at typical conditions. We also pass the jitter tolerance with more than

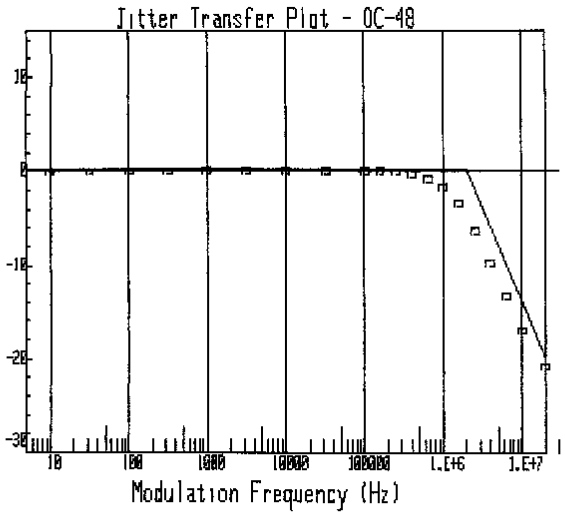

Figure 7: Jitter transfer response

25% overdrive. This measures the ability of the CRU to withstand decreasing amounts of jitter at increasing (jitter) frequencies. The units are in “unit interval” or UI, which is 400 pS for 2.5 Gb/s. For example, at 1 kHz the test equipment applies 4000 pS or 10 UI of jitter. The jitter tolerance plot shows, in squares, the jitter levels versus frequency at which the IC was tested and passed with no data errors. The tests are run with a pseudo random data pattern of length 127, but data integrity is checked for patterns up to 2 billion bits long.

The IC layout is shown in Fig. 8 and its size is 2.5 mm by 2.5 mm. MIM capacitors are used extensively for both loop filtering and for power supply decoupling. The analog portion of the circuit is separated from the digital by large substrate contacts tied to quiet power supply pads. We have plenty of power and ground pins, and we maintain separate buses for the analog, digital and output circuits.

Conclusion

An unaided low power and low cost clock and data recovery circuit for SONET OC-48 applications has been presented. The circuit is implemented in 14GHz bipolar process with three levels of metal. A simple passive filter is used which reduces power consumption and improves the loop stability.

References

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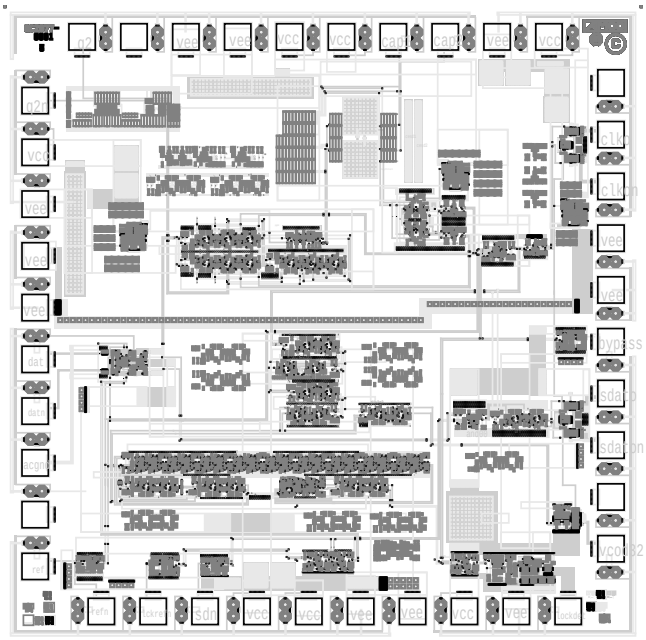

Figure 8: CRU chip plot.